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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/776,084	02/01/2001	Hanan Potash	5625-00100	9421

7590 06/25/2004

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 06/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/776,084	POTASH, HANAN	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2001 and 30 April 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Attorney withdrawal as received 10 September 2001; Withdrawal of Attorney as received on 10 April 2002; and Change of Address as received 30 April 2002.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5, 7-9, and 13 are rejected under 35 U.S.C. 102(b) as being taught by Yue, U.S. Patent Number 5,987,492 (herein referred to as Yue).

6. Referring to claim 1, Yue has taught a computer architecture supporting interleaved execution of multiple threads, comprising:

a. A processor adapted to initiate instructions associated with a thread (Yue column 1, lines 11-40; column 1, line 62 to column 2, line 22; column 4, lines 31-64; and Figure 1);

b. A commutator adapted to sequentially select threads for instruction initiation by the processor (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8); and

c. A cycle allocation table operably coupled to the commutator, comprising an execution time individually allotted to each of the threads (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8).

7. Referring to claim 2, Yue has taught wherein said allotted execution times are not the same for all the threads (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8). In regards to Yue, the allotted execution times are represented by a combination of both the tickets and, as referred to by Yue, the time quantum. If the number of tickets allotted are greater, then the time allotted is greater, since the execution time for that thread is the number of tickets times the time quantum. If the number of tickets allotted are less, then the time allotted is less.

8. Referring to claim 3, Yue has taught wherein the cycle allocation table is capable of being reconfigured during runtime, allowing the execution time allotted to the threads to be independently modified (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8).

9. Referring to claim 4, Yue has taught wherein the configuration of the cycle allocation table and the execution time allotted to the threads is fixed and determined when the processor is designed or manufactured, and cannot be modified during runtime (Yue column 1, line 62 to

column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8).

10. Referring to claim 5, Yue has taught The computer architecture as recited in claim 1, wherein the commutator comprises a circular (i.e., modulo N) counter generating addresses in the cycle allocation table (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8).

11. Referring to claim 7, Yue has taught wherein the processor execution time represents a number of clock cycles (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8).

12. Referring to claim 8, Yue has taught wherein the cycle allocation table contains thread identifiers and the processor execution time allotted to a thread is based on the number of occurrences of its thread identifier in the cycle allocation table (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8).

13. Referring to claim 9, Yue has taught wherein the processor execution time allocated to a given thread is commensurate with the workload of the thread (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8).

14. Referring to claim 13, Yue has taught wherein the processor has no instruction pipeline, and initiates one instruction per clock cycle (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and

Figures 5-8). In regards to Yue, it has not been specified that the system is pipelined and stated that the instructions are executed in a pipelined manner.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 6, 10-12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yue, U.S. Patent Number 5,987,492 (herein referred to as Yue) as applied to claims 1 and 8 above, and in view of Dwyer, III et al., U.S. Patent Number 5,996,068 (herein referred to as Dwyer).

17. Referring to claims 6, 10-12, and 14, Yue has taught a thread identifier and an execution context associated with each thread (Applicant's claim 6) (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8) and wherein there are 16 threads and wherein the cycle allocation table comprises 64 entries (Applicant's claim 14) (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8). In regards to Yue, Yue discloses that there are multiple threads and multiple entries in the table. Multiple threads and entries includes 16 threads and 64 entries. Yue has not taught

a. Wherein the execution context comprises a program counter and register set (Applicant's claim 6).

b. Pipeline control and memory transaction logic, wherein said logic ensures that results of a pipeline operation or memory transaction are directed to the register set belonging to the thread that issued the operation or transaction (Applicant's claim 10).

c. Pipeline/register interlock logic adapted to prevent access to a register awaiting a result from a pending transaction until the result is returned (Applicant's claim 11).

d. Wherein the processor may initiate from 0 to N instructions each clock cycle, where $N \geq 1$ (Applicant's claim 12).

e. Wherein each register set comprises 32 registers (Applicant's claim 14).

18. However, Yue has taught a multi-threaded system (Yue column 1, lines 11-40). Dwyer has taught a multi-threaded system

a. Wherein the execution context comprises a program counter and register set (Applicant's claim 6) (Dwyer column 1, lines 11-22 and column 2, line 46 to column 3, line 6).

b. Pipeline control and memory transaction logic, wherein said logic ensures that results of a pipeline operation or memory transaction are directed to the register set belonging to the thread that issued the operation or transaction (Applicant's claim 10) (Dwyer column 1, lines 11-22 and column 2, line 46 to column 3, line 6).

c. Pipeline/register interlock logic adapted to prevent access to a register awaiting a result from a pending transaction until the result is returned (Applicant's claim 11) (Dwyer column 1, lines 11-22 and column 2, line 46 to column 3, line 6).

d. Wherein the processor may initiate from 0 to N instructions each clock cycle, where $N \geq 1$ (Applicant's claim 12) (Dwyer column 1, lines 11-22 and column 2, line 46 to column 3, line 6).

e. Wherein each register set comprises 32 registers (Applicant's claim 14) (Dwyer column 1, lines 11-22 and column 2, line 46 to column 3, line 6).

19. A person of ordinary skill in the art at the time the invention was made would have recognized that the registers of Dwyer preserve the context and data of a current thread, thereby ensuring the data necessary for the thread to operate properly does not become corrupt. The individual register mapping for each thread allows each thread to have its own set of registers to use and avoid conflict of resources. Also, a person of ordinary skill in the art at the time the invention was made would have recognized that the pipeline of Dwyer enhances processor performance and efficiency. The pipeline allows multiple instructions to be executed at once, since each stage in the pipeline operates on a separate instruction. Consequently, an N stage pipeline is able to operate on N instructions at once during peak performance. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the registers and pipeline of Dwyer in the device of Yue to avoid data corruption and increase processor performance and efficiency.

20. Claims 15-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yue, U.S. Patent Number 5,987,492 (herein referred to as Yue) in view of Dwyer, III et al., U.S. Patent Number 5,996,068 (herein referred to as Dwyer).

21. Referring to claim 15, Yue has taught a method for interleaved execution of a plurality of threads by a compute processor, comprising:

a. Allotting a portion of an execution time of the processor to each thread, wherein a size of the portion may be different for each thread, and wherein the size of each portion comprises an allocation of the execution time (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8); and

b. Executing simultaneously the plurality of threads, with each thread executing for its allotted instruction initiation time (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8).

22. Yue has not taught assigning each thread a program counter, register set and thread identifier. However, Yue has taught a multi-threaded system (Yue column 1, lines 11-40). Dwyer has taught a multi-threaded system assigning each thread a program counter, register set and thread identifier (Dwyer column 1, lines 11-22 and column 2, line 46 to column 3, line 6). A person of ordinary skill in the art at the time the invention was made would have recognized that the registers of Dwyer preserve the context and data of a current thread, thereby ensuring the data necessary for the thread to operate properly does not become corrupt. The individual register mapping for each thread allows each thread to have its own set of registers to use and

avoid conflict of resources. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the registers of Dwyer in the device of Yue to avoid data corruption.

23. Referring to claim 16, Yue has taught wherein said allotting a portion of an execution time comprises placing one or more occurrences of the thread identifier in a cycle allocation table (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8).

24. Referring to claim 17, Yue has taught wherein threads are executed in the order in which their thread identifiers appear in the cycle allocation table (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8).

25. Referring to claim 18, Yue has taught wherein the portion of the execution time allotted to a thread is based on the number of occurrences of its thread identifier in the cycle allocation table (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8).

26. Referring to claim 19, Yue has taught wherein the allotted execution time for a given thread is commensurate with the workload of the thread (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8).

27. Referring to claim 20, Yue has taught wherein the allotted execution time for a given thread is commensurate with the real time requirement of the program to which the thread

belongs (Yue column 1, lines 11-40; column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8).

28. Referring to claim 21, Yue has taught wherein the allotment of execution times to threads may be reapportioned during runtime (Yue column 1, line 62 to column 2, line 22; column 4, lines 31-64; column 6, lines 32-57; column 7, line 18 to column 8, line 30; Figure 1; and Figures 5-8).

29. Referring to claim 22 and 23, Yue has not taught

a. Wherein the result of an operation performed by the computer processor is directed to the register set belonging to the thread that issued the operation or transaction, regardless of which thread is executing when the result becomes available (Applicant's claim 22).

b. Wherein access to a register awaiting a result from a pending transaction is prevented until the result is returned (Applicant's claim 23).

30. However, Yue has taught a multi-threaded system (Yue column 1, lines 11-40). Dwyer has taught a multi-threaded system

a. Wherein the result of an operation performed by the computer processor is directed to the register set belonging to the thread that issued the operation or transaction, regardless of which thread is executing when the result becomes available (Applicant's claim 22) (Dwyer column 1, lines 11-22 and column 2, line 46 to column 3, line 6).

b. Wherein access to a register awaiting a result from a pending transaction is prevented until the result is returned (Applicant's claim 23) (Dwyer column 1, lines 11-22 and column 2, line 46 to column 3, line 6).

31. A person of ordinary skill in the art at the time the invention was made would have recognized that the registers of Dwyer preserve the context and data of a current thread, thereby ensuring the data necessary for the thread to operate properly does not become corrupt. The individual register mapping for each thread allows each thread to have its own set of registers to use and avoid conflict of resources. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the registers of Dwyer in the device of Yue to avoid data corruption.

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Wang et al., U.S. Patent Number 5,771,382, has taught a multi-threaded system.

b. Wang et al., U.S. Patent Number 5,852,731, has taught a multi-threaded system.

c. Doing et al., U.S. Patent Number 6,018,759, has taught a multi-threaded system.

d. Ryo et al., U.S. Patent Number 6,708,197, has taught a multi-threaded system.

e. Sullivan, U.S. Patent Number 5,438,680, has taught a multi-threaded system.

f. Modelski et al., U.S. Patent Number 6,665,755, has taught a multi-threaded, pipelined system.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
24 June 2004

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